REMARKS/ARGUMENTS

In view of the foregoing amendments and the following remarks, reconsideration and allowance of this application is requested. Claims 1-2, 4-9, 15, 22-23 and 39 are now pending, with claim 1 being independent. New claim 39 has been added.

Applicants filed a "Response to Final Office Action" on May 31, 2004 that the Examiner stated failed to place this application in condition for allowance. Applicants request that the previously filed "Response to Final Office Action" be entered and this "Amendment as Submission for Request for Continued Examination" also be entered in the order in which they were filed.

As amended, claim 1 presents a semiconductor device that includes a semiconductor chip with a planar active surface. The planar active surface has an integrated circuit protected by an inorganic overcoat with side walls, the integrated circuit having metallization patterns with a plurality of contact pads. As shown in Figure 2, each of the contact pads 202 has an added conductive layer 205 on the metallization patterns. The added conductive layer 205 has a conformal surface adjacent the semiconductor chip that includes peripheral portions 205a of the inorganic overcoat 203. The added conductive layer 205 also has a planar outer surface 206, 207 covering the side walls of the inorganic overcoat and defining a flat outline substantially parallel to the chip surface (surface of inorganic overcoat 203), the planar outer surface suitable to form metallurgical bonds without melting.

Claim 39 recites that the side walls of the inorganic overcoat are window side walls.

Independent claim 1 stands rejected under 35 U.S.C. § 102(e) as obvious over Lin et al. (6,426,556). Applicants request reconsideration and withdrawal of this rejection for at least the reason that Lin does not describe or suggest a planar outer surface covering the side walls of the inorganic overcoat and defining a flat outline substantially parallel to the chip surface.

Lin, in relevant part, describes a method for creation of metal bumps over surfaces of I/O pads by depositing and etching layers of material. As shown in Figure 9, a passivation layer 32 (corresponding to Applicants' inorganic overcoat 203) is deposited over the surface of layer 29 of dielectric and an opening created in the layer of passivation 32 that aligns with aluminum contact pad 24. Figure 11 shows a cross section of the substrate 10 after the contact pad 24 has

been etched to create opening 36. After depositing different layers as shown in Figures 12-14, Figure 15 shows a cross section after the layer 39 of photoresist and UBM layer 33 shown in Figure 14 have been removed. As shown in Figure 15, the outer surface on passivation layer 32 has side walls. Thus, Lin does not describe or suggest a planar outer surface covering the side walls of the inorganic overcoat/passivation layer and defining a flat outline substantially parallel to the chip surface but rather an outer surface having side walls. As shown in Applicants' Figure 2, the planar outer surface 206, 207 defines a flat outline that covers the side walls of the inorganic overcoat 203. In Lin, metal layer 35, enhanced UBM layer 34, and UBM layer 33 shown in Figure 15 would have to extend in both directions to cover the side walls of passivation layer/inorganic overcoat 32 and create a flat outline substantially parallel to the chip surface.

The planar outer surface covering the side walls of the inorganic overcoat and defining a flat outline substantially parallel to the chip surface provides several advantages. In particular, the flat outline of the planar outer surface substantially parallel to the chip surface and covering side walls around the contact pad reduces stress and cracking along the outer surface and along the bond with the terminal pads of the wiring board, resulting in improved reliability of the device.

For at least the reasons given above, Applicants respectfully submit that claim 1 is patentable over Lin.

Claims 2, 4-9, 15, 22-23, and 39 depend from independent claim 1. Accordingly, Applicants request reconsideration and withdrawal of the rejections for claims 2, 4-9, 15, 22-23, and 39 for at least the reasons discussed above with respect to claim 1.

Claim 2 stands rejected under 35 U.S.C. § 103(a) as obvious over Lin et al. (6,426,556) in view of Kleffner et al. (5,943,597). However, Kleffner fails to remedy the failure of Lin to describe or suggest a planar outer surface covering the side walls of the inorganic overcoat and defining a flat outline substantially parallel to the chip surface. Kleffner describes use of a trench for stress relief in a bumped semiconductor device as shown in Figure 2. The bumped semiconductor device includes a bond pad 12 formed on a semiconductor die 10. A solder bump 22 is formed so as to overlie the bond pad 12 through a UBM conductive layer 18. A stress isolation trench 15 is formed in a first passivation layer 14, so as to surround the solder bump 22. A non-conductive layer 16 of polyimide that is a second passivation layer covers the first

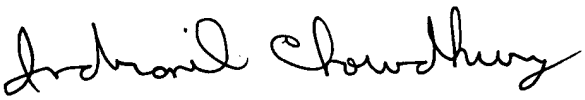
passivation layer 14 up to solder bump 22. Kleffner does not describe or suggest a planar outer surface covering the side walls of the inorganic overcoat/passivation layer and defining a flat outline substantially parallel to the chip surface but rather a curved surface because of the solder bump 22. The curved solder bump 22 does not cover the side walls of passivation layer 16. Accordingly, Applicants request reconsideration and withdrawal of the rejection for at least the reasons discussed above and with respect to claim 1.

Kleffner also does not describe or suggest the limitation given in claim 2 of a non-conductive adhesive layer filling the spaces between the added conductive layers on each of the contact pads. In no part of the Kleffner reference is non-conductive layer 16 described as an adhesive layer over the overcoat layer 14. Kleffner also does not show in Figure 2 or describe or suggest in any other part of the reference the non-conductive layer filling the spaces between the added conductive layers. Thus, Applicants request reconsideration and withdrawal of the rejection of claim 2 for this further reason.

Claims 22 and 23 stand rejected under 35 U.S.C. § 103(a) as obvious over Lin et al. (6,426,556) in view of Elenius et al. (6,287,893). However, Elenius fails to remedy the failure of Lin to describe or suggest a planar outer surface covering the side walls of the inorganic overcoat and defining a flat outline substantially parallel to the chip surface. Elenius describes, as shown in Figure 2, a chip scale package 8 for a flip chip integrated circuit 10 that includes a redistribution conductive layer 30 upon the upper surface of a semiconductor wafer 14 for simultaneously attaching to solder balls 28 as well as with the conductive bond pad 18 of the underlying integrated circuit. Elenius does not describe or suggest a planar outer surface covering the side walls of the inorganic overcoat and defining a flat outline substantially parallel to the chip surface but rather an outer surface interrupted by a large sphere-like solder ball as shown in Figures 2 and 3 for attachment to a circuit board. Accordingly, Applicants request reconsideration and withdrawal of the rejection for at least the reasons discussed above and with respect to claim 1.

In view of these remarks and amendments, Applicants submit that this application is now in condition for allowance and the Examiner's prompt action in accordance therewith is respectfully requested. The Commissioner is authorized to charge any additional fees and/or credit any overpayment to Deposit Account 20-0668 of Texas Instruments Incorporated.

Respectfully submitted,



Indranil Chowdhury
Attorney for Applicants
Reg. No. 47,490

W. James Brady, III
Texas Instruments Incorporated
P.O. Box 655474, MS 3999
Dallas, TX 75265
(972) 917-4371